WHAT IS CLAIMED IS:

1. A nonvolatile memory comprising:

a nonvolatile memory element having at least first and second terminals;

a voltage source coupled to at least one terminal to provide a first voltage during a first time period, said first voltage being less than the voltage required to for electrons to flow to or from a floating gate of the nonvolatile memory element; and

a charge pump circuit coupled to said at least one terminal, the charge pump circuit including at least one capacitor that receives a second voltage during a second time period, and in accordance therewith, further increases the voltage on said terminal so that electrons flow to or from the floating gate of the nonvolatile memory element.

2. The nonvolatile memory of claim 1 further comprising a plurality of transistors coupled to the first terminal, wherein during the second time period one or more of the plurality of transistors receives a third voltage so that the difference between the voltage on the first terminal and the third voltage is less than the breakdown voltage of the one or more transistors.

3. The nonvolatile memory of claim 2 wherein the first terminal, the at least one capacitor, and at least one of the plurality of transistors comprise doped active regions that are coupled together.

4. The nonvolatile memory of claim 1 wherein the floating gate is coupled to the gate of a MOS transistor for generating a current when the floating gate is at a first voltage and turning off said current when the floating gate is at a second voltage.

5. The nonvolatile memory of claim 4 further comprising a latch having a first latch node coupled to said current and a second latch node coupled to a reference current, wherein the latch takes on a first state when said current is greater than said reference current, and said latch takes on a second state when said current is less than said reference current.

6. The nonvolatile memory of claim 1 further comprising a redundant nonvolatile memory element and a redundant charge pump circuit.

7. The nonvolatile memory of claim 1 wherein the nonvolatile memory element and the at least one capacitor comprise doped active regions, an oxide layer, and a polysilicon layer.

8. The nonvolatile memory of claim 1 wherein the nonvolatile memory element comprises a nonvolatile memory device coupled to a capacitor.

9. The nonvolatile memory of claim 8 wherein the nonvolatile memory device is a tunneling capacitor.

10. A nonvolatile memory comprising:

a nonvolatile memory element having at least first and second terminals and a floating gate; and

one or more capacitors coupled in series to the first terminal,

wherein during a first time period, a first voltage is coupled to the first terminal and a second voltage is coupled to the second terminal, the first voltage being greater than the second voltage, and during a second time period following the first time period, a third voltage is coupled through at least one of the capacitors to the first terminal, the third voltage further increasing the voltage on the first terminal so that electrons flow to or from the floating gate.

11. The nonvolatile memory of claim 10 wherein electrons move from the floating gate to the first terminal to erase the nonvolatile memory element.

12. The nonvolatile memory of claim 10 wherein electrons move from the first terminal to the floating gate to program the nonvolatile memory element.

13. The nonvolatile memory of claim 10 further comprising a plurality of transistors coupled to the first terminal, wherein during the second time period one or more of the plurality of transistors receives a fourth voltage so that the difference between the voltage on the first terminal and the fourth voltage is less than the breakdown voltage of the one or more transistors.

14. The nonvolatile memory of claim 13 wherein the first terminal, at least one of said capacitors, and the one or more of the plurality of transistors comprise doped active regions that are coupled together.

15. The nonvolatile memory of claim 10 further comprising a first voltage source that provides the first voltage during the first time period and a second voltage source that provides the third voltage during the second time period following the first time period.

16. The nonvolatile memory of claim 15 wherein the first voltage source increases approximately linearly to the first voltage during the first time period, and the second voltage source increases approximately linearly to the third voltage during the second time period, and in accordance therewith, the voltage on the first terminal of the nonvolatile memory element increases approximately linearly from an initial voltage to an intermediate voltage during the first time period, and increases approximately linearly from the intermediate voltage to a final voltage during the second time period.

17. The nonvolatile memory of claim 10 further comprising first and second voltage sources, the first voltage source providing a two-part voltage signal including the first voltage during the first time period and a fourth voltage during the second time period, and the second voltage source providing a one-part voltage signal during the second time period.

18. The nonvolatile memory of claim 10 wherein the nonvolatile memory element comprises a nonvolatile memory device having a floating gate coupled to a first capacitor.

19. The nonvolatile memory of claim 18 further comprising:

a second capacitor coupled to the first terminal;

a third capacitor coupled between the first and second capacitors;

a first voltage source coupled to the first terminal, the first voltage source providing the first voltage to the first terminal during the first time period; and

a second voltage source coupled to a node between the second and third capacitors, the second voltage source providing the third voltage to the second capacitor during the second time period to further increase the voltage on the first terminal.

20. The nonvolatile memory of claim 19 wherein the first voltage source comprises a first MOS transistor having a gate coupled to a control voltage, a drain coupled to the first terminal, and a source coupled to a fourth voltage.

21. The nonvolatile memory of claim 20 wherein the first voltage source further comprises a second MOS transistor having a gate coupled to the control voltage, a drain coupled to the first and third capacitors, and a source coupled to receive the second voltage.

22. The nonvolatile memory of claim 21 further comprising a latch having a first latch node coupled to source of the first MOS transistor and a second latch node coupled to the source of the second MOS transistor.

23. The nonvolatile memory of claim 19 wherein the floating gate is coupled to the gate of a MOS transistor for generating a current when the floating gate is at a first voltage and turning off said current when the floating gate is at a second voltage.

24. The nonvolatile memory of claim 23 further comprising a latch having a first latch node coupled to said MOS transistor to receive said current and a second latch node coupled to a reference current, wherein the latch takes on a first state when said current is greater than said reference current, and said latch takes on a second state when said current is less than said reference current.

25. A method of operating a nonvolatile memory comprising:

during a first time period, coupling a first voltage to a first terminal of a nonvolatile memory element and coupling a second voltage to a second terminal of the nonvolatile memory element, wherein the first voltage is greater than the second voltage; and

during a second time period, coupling a third voltage through at least one capacitor to the first terminal, the third voltage further increasing the voltage on the first terminal so that electrons flow to or from a floating gate in said nonvolatile memory element.

26. The method of claim 25 wherein a plurality of transistors are coupled to the first terminal, and wherein during the second time period one or more of the plurality of transistors receives a fourth voltage so that the difference between the voltage on the first terminal and the fourth voltage is less than the breakdown voltage of the one or more transistors.

27. The method of claim 26 wherein during the first time period, the first voltage is coupled to the first terminal through a first transistor from said plurality of

transistors, and during the second time period, the fourth voltage is received by said first transistor so that the voltages on the first transistor do not exceed the first transistors breakdown voltage.

28. The method of claim 27 wherein the first voltage is coupled to the gate of a MOS transistor, the source of the MOS transistor is coupled to a fourth voltage and the drain of the MOS transistor is coupled to the first terminal.

29. The method of claim 28 wherein the fourth voltage is the voltage output of a latch.

30. The method of claim 25 wherein the nonvolatile memory element comprises nonvolatile memory device coupled to a first capacitor, and the second voltage is coupled through the first capacitor to the floating gate terminal, and electrons flow from the floating gate terminal to the first terminal during the second time period so that the voltage on the floating gate increases from a first voltage to a second voltage after the first and second time periods.

31. The method of claim 25 wherein the nonvolatile memory element comprises nonvolatile memory device coupled to a first capacitor, and the first voltage is coupled through the first capacitor to the floating gate terminal during the first time period, and electrons flow from the first terminal to the floating gate terminal during the second time period so that the voltage on the floating gate decreases from a first voltage to a second voltage after the first and second time periods.

32. The method of claim 25 wherein during the first time period, the voltage on the first terminal of the nonvolatile memory element is increased to a voltage below that at which electrons will flow to the floating gate, and during the second time period, the voltage on the first terminal of the nonvolatile memory element is increased to a voltage above that at which electrons will flow to the floating gate.

33. The method of claim 25 wherein during the first time period the voltage on the first terminal increases approximately linearly to the first voltage, and during the second time period the voltage on the first terminal increases approximately linearly to a final voltage sufficient to allow electrons to flow to or from the floating gate.

34. The method of claim 25 further comprising:

sensing a voltage on the floating gate, and in accordance therewith, generating a first current; and

comparing the first current to a reference current to determine voltage on the floating gate.